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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,327	01/09/2004	Helmut Preisach	Q78982	7254

72875   7590   01/10/2008

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EXAMINER
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ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
01/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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		Application No.	Applicant(s)
Office Action Summary		10/753,327	PREISACH, HELMUT
		Examiner	Art Unit	
		Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>19 October 2007</u>.

2a) ☒ This action is **FINAL.**   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1 - 16* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1 - 2, 4 - 14, 16* is/are rejected.

7) ☒ Claim(s) *3 and 15* is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☒ All b)☐ Some * c)☐ None of:

   1. ☒ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Response to Arguments

1.   The Examiner has accepted changes to the claims made in response to the
claim objections.

2.   Applicant's arguments filed 10/19/2007 have been fully considered but they are
not persuasive.

Argument: Applicant argued that Smith does not disclose that the detection of the bit
rate is done by the retiming circuit 34 (Remarks 10/19/2007, page 7, last paragraph)
and that Maione also does not disclose the same (Remarks 10/19/2007, page 8, 2nd last
paragraph).

Response: Examiner respectfully disagrees. Firstly, Applicant has stated that there is no
specific teaching in Smith, that detection of a higher bit rate or a lower bit rate is made
at the retiming circuit 34 (Remarks 10/19/2007, page 8, 1st 2 lines) and then later has
himself admitted that there is bit rate detection done in the retiming circuit 34 (Remarks
10/19/2007, page 8, 2nd last paragraph, 1st 2 lines). If Applicant contends that Smith
does not teach detection of the bit rates in element 34, Maione clearly shows that bit
rate detection is done within the decision and timing circuit 300 (Fig. 3, element 310).
The phase lock, freq-lock, timing recovery module 303, which includes element 310,
corresponds to the clock and data recovery module in Applicant's invention. Maione
was used in the rejection of claim 2 and since he shows it more clearly than Smith,
Examiner is using Maione for this limitation in this Office Action to address the
amendments in claim 1.

Argument: Applicant argued that the "terminal EA is not an output of the equalizer EGA

... " (Remarks 10/19/2007; page 9, 4th paragraph).

Response: Examiner respectfully disagrees. Claim 4 simply states "a test loop

controllably connected from the output to the input of the regenerator". Carriere clearly

discloses a test loop in which the output is fed back to the input (column 11, lines 13 –

18, 26 – 34; wherein the test loop feeds the signal from the output to the input).

Argument: Applicant argued that Smith is directed to old LAN technology whereas the

invention is geared towards a higher date rate than in LAN (Remarks 10/19/2007, page

10, middle paragraph).

Response: Even though data rates may be different, the concept is the same and one of

ordinary skill in the art can easily adapt Smith's disclosure to a higher data rate.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 1, 2, 12, 13 rejected under 35 U.S.C. 103(a) as being unpatentable over

Smith et al. (US 6,233,077) in view of Maione et al. (US 4,019,048).

Regarding claim 1, Smith discloses an electrical signal regenerator (column 3, lines 51

– 52) comprising:

an equalizer (Fig. 4, element 51; column 4, lines 60 - 67);

a clock data recovery circuit (Fig. 4, element 34; column 5, line 1 – column 6, line 16);

and a switch (Fig. 4, element 60; column 6, lines 17 – 23; wherein the switch is the

multiplexer 60 that selects one of the two inputs);

wherein said switch is operable to either connect the clock data recovery circuit to an

output of the electrical signal generator when an input signal of higher bitrate multiplex

signal is present or bypass the data recovery or bypass the clock data recovery circuit

and connect the equalizer to the output of the electrical signal generator when an input

signal of a lower bitrate multiplex signal is present (Fig. 4, element 60; column 6, lines

17 – 23; wherein the switch is the multiplexer 60 that selects one of the two inputs

according to one of the two data rates, 4MB/s or 16 MB/s).

Smith does not clearly disclose whether the clock and data recovery circuit calculates

the bit rate.

Maione discloses the clock data recovery circuit comprises a detector for detecting the bit rate of the input signal (column 8, lines 51 – 61; Fig. 3, element 310; wherein the bit rate detection is done by extracting the frequency of the data pulse stream [last 2 lines]).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Maione, in the system of Smith because this would provide a means for detecting the bit rate of the input signal, as disclosed by Maione.

Claim 2 is analyzed as the corresponding limitation in claim 1.

Regarding claim 12, Smith discloses a method of transmitting an electrical signal having either a first or a second bit rate wherein the first bit rate is higher than the second bit rate (Abstract; column 2, lines 15 – 20; column 3, lines 35 – 37; Fig. 4, element 60, which selects one of the two data rates);

said method comprising the steps of transmitting said electrical signal via a signal path (column 3, lines 35 – 37);

detecting the bit rate of said electrical signal received from the signal path (Abstract, line starting with "The associated …"; column 3, lines 21 – 26; column 5, lines 48 – 50;

column 10, lines 5 – 8; wherein the bit rate is known from the frequency at which the resonance occurs);

in the case the electrical signal has the first bit rate, performing a first regeneration of said electrical signal and then performing a second regeneration and in the case the signal has the second bit rate, performing said first regeneration of said signal, only (Fig. 4, element 60 which selects either the output of the equalizer or the output of the clock recovery circuit 34 [after equalization]).

Regarding claim 13, Smith discloses first signal regeneration is an electrical equalization (Fig. 4, element 51; column 4, lines 60 - 67) and wherein said second signal regeneration is a clock data recovery (Fig. 4, element 34; column 5, line 1 – column 6, line 16).

5.   Claims 4 , 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (US 6,233,077) in view of Maione et al. (US 4,019,048) and further in view of Carriere (US 5,504,778).

Regarding claim 4, Smith does not disclose a test loop from output to input.

In the same field of endeavor, however, Carriere discloses a test loop controllably

connectable from the output to the input of the regenerator (column 11, lines 13 – 18, 26

– 34; wherein the test loop feeds the signal from the output to the input).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Carriere, in the system of

Smith because this would allow a loop test to be performed, as is well known in the art.

Regarding claim 14, Smith does not disclose a test loop from output to input.

In the same field of endeavor, however, Carriere discloses a static test signal is fed via

the test loop to an input of the equalizer while no external signal is input to the input of

the equalizer (column 11, lines 13 – 18, 26 – 34; wherein the test loop feeds the signal

from the output to the input when no input signal is present).

6.   Claim 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Smith et al. (US 6,233,077) in view of Maione et al. (US 4,019,048) and further in view

of Roberts (US 6,067,180).

Regarding claim 5, Smith does not disclose that the analog equalizer is a tapped delay

line.

In the same field of endeavor, however, Roberts discloses equalizer being an analogue

equalizer comprising a tapped delay line (Fig. 6; column 3, lines 10 – 11, 17 - 31).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Roberts, in the system of Smith because this would provide a means for equalization of the received signal, as is well known in the art.

Regarding claim 6, Smith does not disclose the equalizer has a first and second tap, with the first tap having a higher delay than the second tap and the two signals being connected to an adder/subtractor.

In the same field of endeavor, however, Roberts discloses the analogue equalizer comprising a first tap and a second tap, the first tap having a higher delay than the second tap, both taps being connected to a adder-subtractor for generating a difference signal (column 3, lines 17 - 31; Fig. 6; wherein the analog equalizer is the one used in the optical domain).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Roberts, in the system of Smith because this would provide a means for equalization of the received signal, as is well known in the art.

Regarding claim 7, Smith does not disclose the signal ratio between the two taps is adjustable.

In the same field of endeavor, however, Roberts discloses the signal ratio between the

two taps is adjustable (column 3, lines 17 – 31; wherein the adjustable taps is the filter

weights that are controlled to provide an adaptive equalizer).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Roberts, in the system of

Smith because this would provide a means for equalization of the received signal, as is

well known in the art.

7.   Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et

al. (US 6,233,077) in view of Maione et al. (US 4,019,048) and further in view of

Roberts (US 6,067,180) and Townsend et al. (US 5,323,423).

Regarding claim 8, Smith does not disclose that peak detectors determine the ratio.

In the same field of endeavor, however, Townsend discloses the signal ratio between

the two taps is adjustable, and wherein the ratio is determined by two peak detectors

(Fig. 2, elements 20a, 20b, 24; column 2, lines 14 – 58; wherein the equalizer is the

variable filters 20a and 20b and the peak detectors [lines 41 – 46] are used to determine

the pulse width adjustment that in turn is used to adjust the variable filter parameters).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Townsend, in the system of

Smith because this would allow the equalizer parameters to be adjusted based on a

measure of the distortion in the signal present, in Townsend's case the measure being

the pulse width value).

8.   Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et

al. (US 6,233,077) in view of Maione et al. (US 4,019,048) and further in view of

Feustel et al. (US 5,552,962).

Regarding claim 9, Smith discloses a signal regenerator (column 3, lines 51 – 52)

comprising an equalizer (Fig. 4, element 51; column 4, lines 60 - 67) and a clock data

recovery circuit (Fig. 4, element 34; column 5, line 1 – column 6, line 16)

and a switch (Fig. 4, element 60; column 6, lines 17 – 23; wherein the switch is the

multiplexer 60 that selects one of the two inputs) said switch is operable to either

connect the data recovery circuit to an output of the electrical signal generator when an

input signal of a higher bit rate multiplex signal is detected or to bypass the data

recovery circuit and connect the equalizer to the output electrical signal generator when

an input signal of a lower bit rate multiplex signal is detected (Fig. 4, element 60;

column 6, lines 17 – 23; wherein the switch is the multiplexer 60 that selects one of the

two inputs according to one of the two data rates, 4MB/s or 16 MB/s).

Smith does not disclose a network element comprising internal signal paths terminated by an electrical signal generator and also does not clearly disclose that the clock and data circuit determines the bit rate.

Maione discloses the clock data recovery circuit comprises a detector for detecting the bit rate of the input signal (column 8, lines 51 – 61; Fig. 3, element 310; wherein the bit rate detection is done by extracting the frequency of the data pulse stream [last 2 lines]).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Maione, in the system of Smith because this would provide a means for detecting the bit rate of the input signal, as disclosed by Maione.

In the same field of endeavor, however, Feustel discloses a network element (Fig. 6, elements 60, 61; column 3, lines 31 - 38) comprising internal electrical signal paths (column 1, lines 22 - 32), wherein at least part of said paths are terminated by an electrical signal regenerator (column 1, lines 22 – 32).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Feustel, in the system of Smith because this would allow regeneration of signals that are distorted by the transmission channel, as is well known in the art.

9.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et

al. (US 6,233,077) in view of Maione et al. (US 4,019,048) and further in view of

Feustel et al. (US 5,552,962) and Boulais et al. (US 20030002498).

Regarding claim 10, the combined invention of Smith and Feustel does not disclose a

switching matrix comprising switch modules connected by cables and regenerator.

In the same field of endeavor, however, Boulais discloses an optical cross connect

comprising an electrical space switching matrix, said matrix comprising a number of

switch modules (page 1, paragraphs 2 – 4, 8) being interconnected by means of

internal electrical cables (page 2, paragraphs 23), an electrical signal regenerator is

coupled to one end of each internal electrical cable in front of a switching module (Fig.

3, element 38; which is the regenerator connected before the TX module which passes

the data onto the various transmission lines).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Boulais, in the combined

system of Smith and Feustel because this would enable communication of signals in a

optical network.

10.   Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et

al. (US 6,233,077) in view of Maione et al. (US 4,019,048) and further in view of

Feustel et al. (US 5,552,962), Boulais et al. (US 20030002498), Zwan et al. (US

5,991,270) and Yeates (US 5,278,404).

Regarding claim 11, the combined invention of Smith, Feustel and Boulais does not

disclose a test signal at each output port and that the regenerators raise an alarm when

a valid input signal is not valid.

In the same field of endeavor, however, Zwan discloses matrix modules being adapted

to output a test signal at each unused output port (column 12, line 46 – column 13, line

34).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Zwan, in the combined system

of Smith, Feustel and Boulais because this would test procedure s to be conducted, as

is well known in the art.

In the same field of endeavor, however, Yeates discloses the electrical signal

regenerators are adapted to raise an alarm when neither a test signal nor a valid input

signal is detected (column 2, lines 46 – 49; Fig. 2, element 44; column 3, line 47 –

column 4, line 15; wherein the absence of a valid input or test signal is interpreted as a

loss transmission).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Yeates, in the combined

system of Smith, Feustel and Boulais because this would allow one to know that there is

a loss of input signal, as disclosed by Yeates.

11.   Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith

et al. (US 6,233,077) in view of) in view of Maione et al. (US 4,019,048) and further in

view of Applicant Admitted Prior Art (hereafter referred to as AAPA).

Regarding claim 16, Smith does not disclose the data rates of 10 Gbits/s and 2.7

Gbits/s.

In the same field of endeavor, however, AAPA discloses the higher bit rate is

approximately 10 Gbit/s and the lower bit rate is approximately 2.7 Gbits/s

(Specification, page 1, last paragraph; wherein the Applicant has admitted that the ITU-

T G.709 specification has 3 levels of hierarchy with bit rates of 2.7 and 10 Gbps).

Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by AAPA, in the system of Smith,

because this would allow support of various bit rates, as disclosed by AAPA prior art.

Allowable Subject Matter

12.   Claim 3, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

13.   The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to regeneration, equalization and clock recovery:

Maione et al. (US 4,019,048) discloses Regenerator for an optical transmission system.

Russer et al. (US 4,060,739) discloses circuit arrangement for amplifying pulsed signals.

Bowen (US 4,498,167) discloses a TDM Communication system that uses regeneration and clock recovery.

Bickers (US 4,761,797) discloses a Flexible regenerator.

Mantovani (US 4,839,905) discloses a Multirate automatic equalizer.

Conclusion

14.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Contact Information

15.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Adolf DSouza whose telephone number is 571-272-

1043. The examiner can normally be reached on Monday through Friday from 8:00 AM

to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David Payne can be reached on 571-272-3024. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

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